

## Complete Multi-Port 4.5 Gbps D-PHY CSI-2/DSI-2 Generator

An Introspect 8-lane MIPI D-PHY generator enables developers of high-bandwidth CSI-2 or DSI-2 applications to completely verify their designs and characterize their performance margins. The highly integrated form factor and the single software environment allow for unprecedented ease of use when it comes to creating multi-port CSI-2 or DSI-2 transmissions. Features include image importing, video sequence generation, and image splitting between MIPI ports.



### Key Features

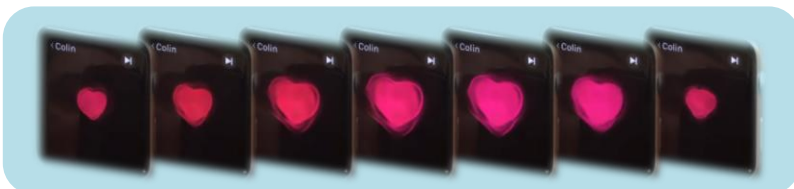
- **Data rates:** continuous operating range from 80 Mbps to 4.5 Gbps per lane
- **Lanes:** 8 data lanes and 2 clock lanes
- **PHY features:** complete D-PHY 1.2 and 2.0 signaling capability, include LP, HS, and BTA
- **DSI-2 protocol features:** command mode and video mode generation, tearing effect triggers, variable video timing, DCS command insertion
- **CSI-2 protocol features:** lane distribution, embedded data, and variable frame timings

### Key Benefits

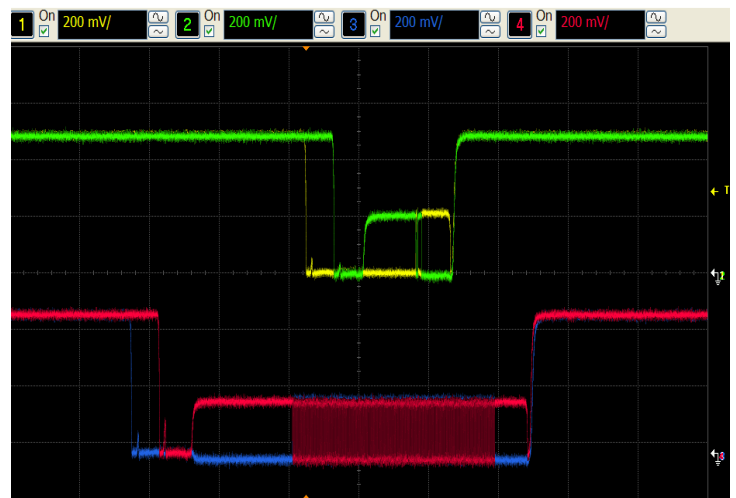
- **Self-contained:** solution with two 4-lane MIPI D-PHY ports in an ultra compact form factor
- **Flexible:** solution featuring arbitrary video sequence generation, CSI-2/DSI-2 protocol support, and real time voltage controls
- **Automated:** scripting capability ideal for debug tasks, verification and full-fledged production screening of devices and system boards
- **Easy development:** based on the Introspect ESP software environment and associated vector generation tools

Params	Log	Results
Components		
dphyColorBarPattem1		00011101
dphyParameters1	dphyParameters1 properties (class: MpiDphyParameters)	
mipiDphyGenerator1		
	setBits	
	tHpxDuration	80.0
	tHsPrepareDuration	(5.0, 60.0)
	tHsZeroDuration	(10.0, 145.0)
	tHsTrailDuration	(8.0, 60.0)
	tClockPrepareDuration	(0.0, 80.0)
	tClockZeroDuration	(0.0, 300.0)
	tClockTrailDuration	(0.0, 80.0)
	tClockPreDuration	(32.0, 0.0)
	tClockPostDuration	(60.0, 60.0)

Arbitrary D-PHY global timing parameters



Deep vector memory allows for transmission of real video sequences



High performance signaling

## General Specifications

Feature	Description	Benefit
Physical Layer	D-PHY	Allows for low-power, high-speed, and bus turn around (BTA) communication
Protocol Layer	CSI-2 / DSI-2	Flexible software allows for closely tracking the rapid MIPI Alliance protocol evolution
Number of Data Lanes	8 (+ 2 Clock Lanes)	Tests high resolution camera or display modules
Data Rate Range	80 Msps – 4.5 Gbps	Provides a future-proof investment for next generation device data rates

## Electrical Specifications

Feature	Description	Benefit
HS Voltage Range ( $ V_{od} $ )	20 mV – 400 mV	Allows testing receiver voltage sensitivity during protocol transmissions
HS Voltage Resolution	<10 mV	Enables executing characterization sweeps
LP Voltage Range	-100 mV – 1600 mV	Allows for covering minimum voltage tests during protocol transmissions
Per Wire Skew Injection Range	-1 UI – 1 UI	Enables executing characterization sweeps

## Pattern Specifications

Feature	Description	Benefit
Preset Patterns	HS-only PRBS polynomials, LP-only preset patterns, PRBS packet loops	Reduces the amount of programming required
User Pattern Memory	Arbitrary video sequences in up to 4 Gbyte of memory space	Provides large test coverage on the most advanced high-definition applications
Multi-Port Features	Software-based image splitting, independent port control, or replication of data on two ports	Provides flexibility to operate in multiple user environments